

FIG. 1

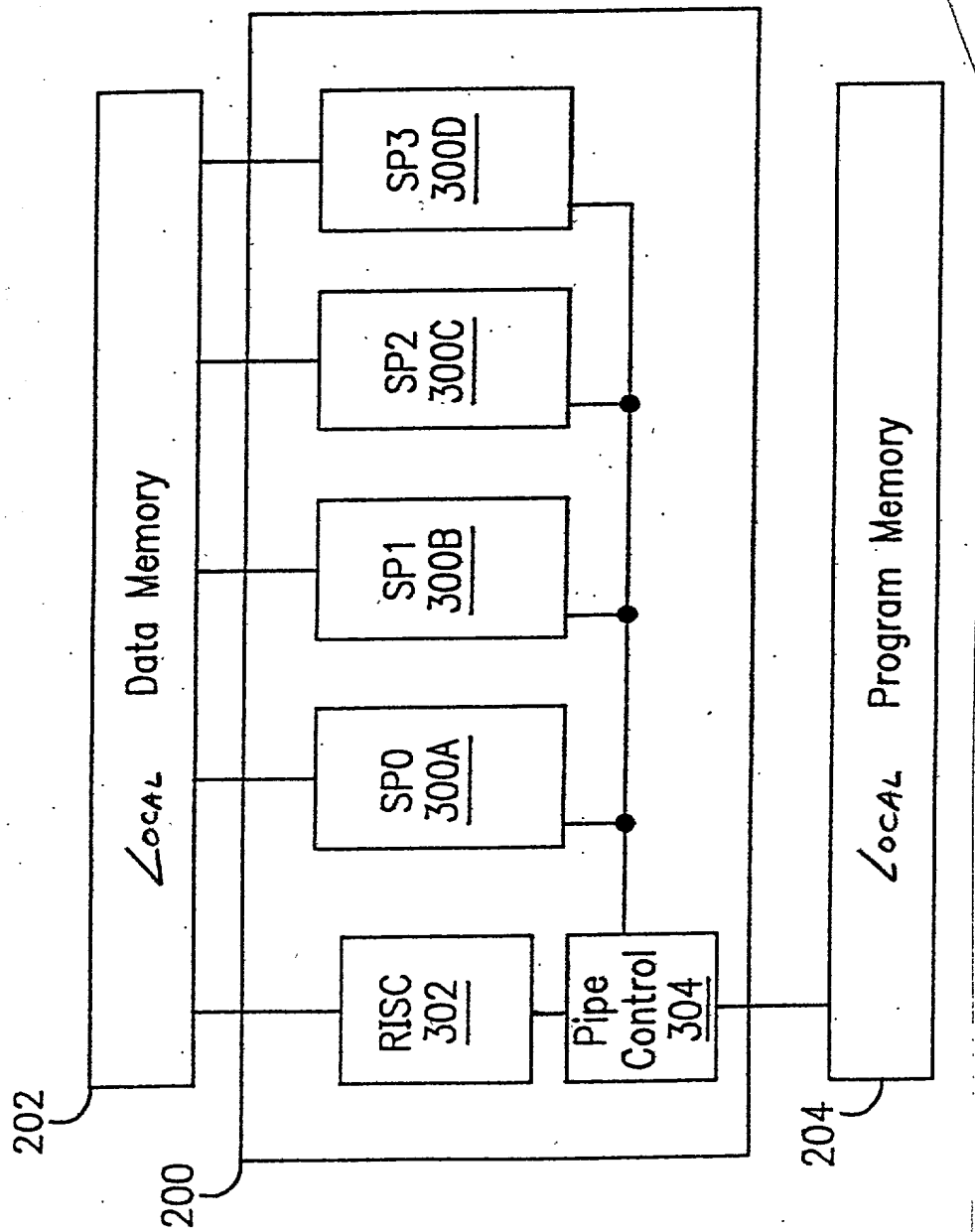


FIG. 2

LWLN					SEQUENCE #	START ADDRESS					FF...F	RWLN
.	.	.	.	.	.						.	.
.	.	.	.	.	.						.	.
.	.	.	.	.	.						.	.
LWL4	18	19	1A	1B						1C	1D	1E
LWL3	10	11	12	13						14	15	16
LWL2	08	09	0A	0B						0C	0D	0E
LWL1	00	01	02	03						04	05	06
	LWBC1	LWBC2	LWBC3	LWBC4						RWBC1	RWBC2	RWBC3

404L

404R

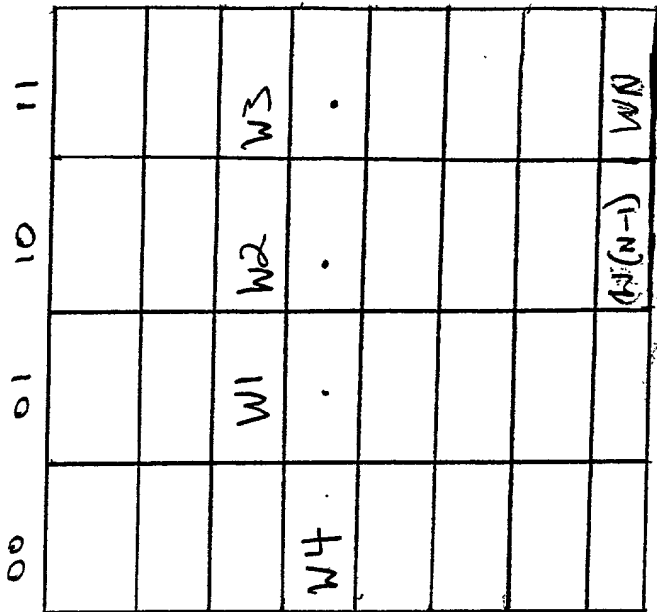
OFF BOUNDARY ROW

Address Decoder

402

FFG  
M  
A

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## HARDWARE DESIGNER'S VIEW

LA b

33

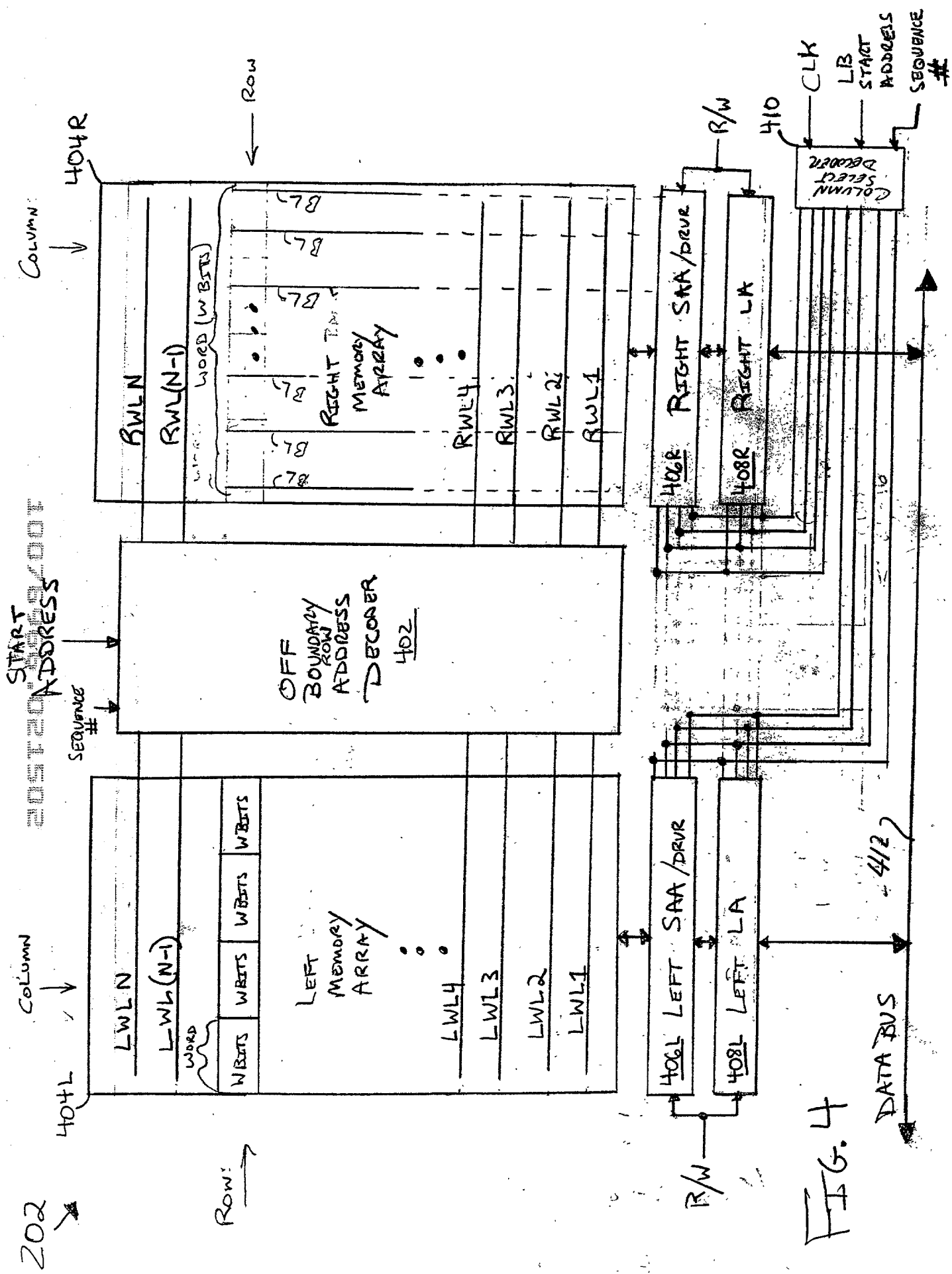


FIG. 4

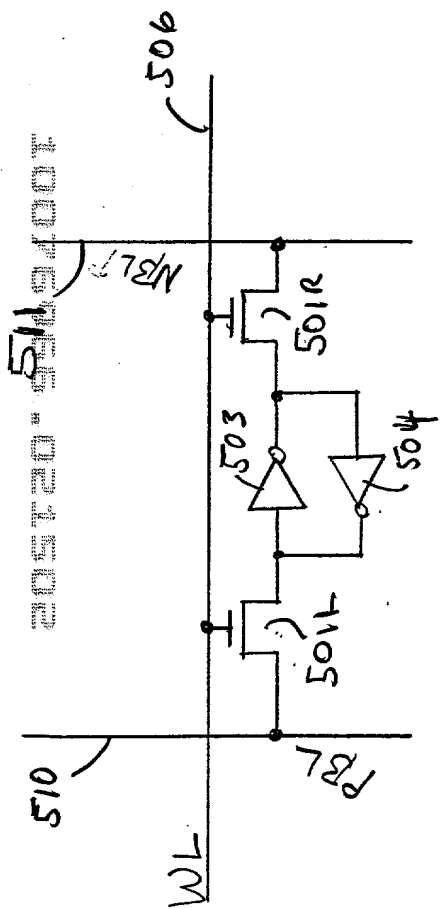


FIG. 5A

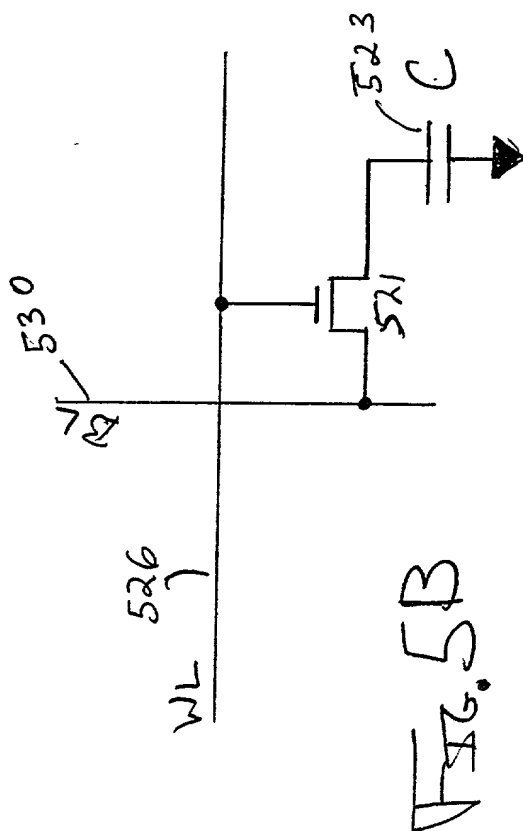


FIG. 5B

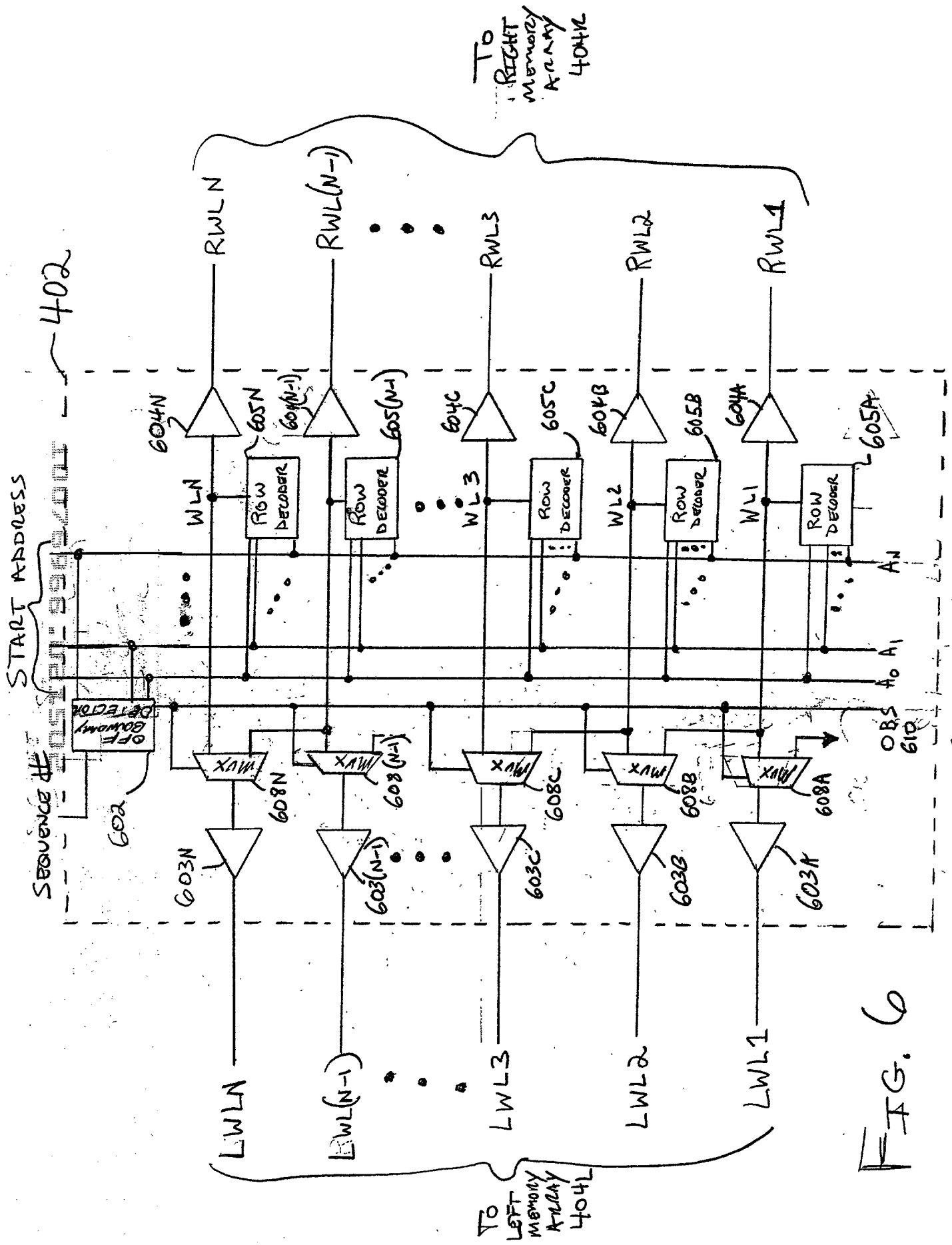


FIG. 6